REMARKS

Reconsideration is requested.

In this response, claims 17, 30, and 32-35 have been amended. Claims 1-16 have been withdrawn from consideration. Claims 17-35 remain pending.

In the instant Office Action, claims 17, 30, and 32-35 have been objected to for minor informalities; claims 17-35 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite; and claims 17-35 were rejected under 35 U.S.C.102(b) as being anticipated by U.S. Patent No. 5,508,937 to Abato (hereinafter "Abato").

Claims 17, 30, and 32-35 have been amended to overcome the objections set forth in the Office Action. It is believed that the objections have now been overcome. Similarly, claims 17, 30, and 32-35 have been amended and are therefore believed to have overcome 35 USC 112, second paragraph rejections.

Applicants respectfully traverse rejection of claims 17-35 under 35 USC §102(b) as being anticipated by Abato. The Office Action asserts that Abato teaches all the elements of claim 17 and refers to various portions of Abato in support of such assertion. Applicants traverse the rejection in view of the following:

> Under MPEP §2131:
>
> > To anticipate a claim, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the ... claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 17 recites a method for incremental statistical timing analysis of an electrical circuit, comprising (a) conducting an initial statistical timing analysis and saving one or more arrival **tightness probabilities** ...; (b) creating a change list based on the changes to the electrical circuit and one or more statistical timing queries, and assigning levelization parameters to each edge of the

timing graph; (c) conducting incremental statistical forward propagation of arrival times and **tightness probabilities** ...; ... (d) conducting incremental statistical reverse propagation of required arrival times and required arrival **tightness probabilities** on a selected edge of the timing graph....(Emphasis Added)

Abato merely discloses an incremental timing analyzer for selectively performing timing analysis on a revised electronic circuit design resulting from one or more modifications to an initial electronic circuit design having input nodes, output nodes, and active elements.

At the outset, Applicant notes that the Examiner has confused "tightness probabilities" as recited in the claimed invention with Abato's "Arrival Time Recomputation List (ATRL) and "Required Time Recalculation List (RTRL)". These are further explained below:

The Office Action asserts that Abato's col. 1, lines 58-63 teach conducting an initial statistical timing analysis and saving one or more arrival tightness probabilities and one or more required arrival tightness probabilities. This assertion is respectfully traversed. Abato, at col. 1, lines 58-63, merely discloses that "the propagated arrival and required times may be single numbers, ranges of values, statistical distributions, ...or a parametric equation representing arrival/required times as a function of some design variable" and nothing more. It fails to teach or suggest conducting an initial statistical timing analysis and saving one or more arrival tightness probabilities and one or more required arrival tightness probabilities as recited in claim 17.

Further, Abato's col. 7, line 67 to col. 8, line 25 merely disclose ATRL and RTRL as noted above. Abato's arrival time recomputation list (ATRL) is simply a list of timing points or timing nodes whose arrival time must be recalculated due to changes in the circuit. Also see Abato's col. 9, lines 35-52. This list is preferably stored in a manner that is indexed by level number (See Abato's Figure 6). The ATRL and RTRL lists indicate that the timing points or timing nodes must be updated or recomputed based

purely on topological reasoning.

Unlike Abato, claim 17 recites *conducting an initial statistical timing analysis and saving* one or more arrival **tightness probabilities** ...; (b) creating a change list based on the changes to the electrical circuit and one or more statistical timing queries, and assigning levelization parameters to each edge of the timing graph; (c) conducting incremental statistical forward propagation of arrival times and **tightness probabilities** ...; (d) conducting incremental statistical reverse propagation of required arrival times and required arrival **tightness probabilities** on a selected edge of the timing graph....

The arrival tightness probability as in the claimed invention provides a convenient measure to estimate the impact of each input in determining the arrival time of the output of a gate. See page 16, lines 15-18 of the present specification. Thus, in a timing graph, by examining the arrival tightness probabilities of the edges incident upon a node, one can immediately deduce which of these edges determined the arrival time of the node by inspecting tightness probabilities. Similarly, by examining the required tightness probabilities, one can immediately deduce which edges determine the required time of the node. Page 16 of the present specification provides further details.

When conducting incremental timing analysis, a change made to a circuit propagates through a timing graph, and tightness probabilities, as in the claimed invention, indicate when one can stop recomputing timing quantities. For example, if only one input of a gate has a changed arrival time, and the edge of the graph from that input to the output has a zero tightness probability before and after the change to the circuit, then the fanout cone of that gate need not be recomputed. See page 14, lines 1-10 for further details. Also see Fig. 3.

Arrival tightness probabilities is a timing-based determination of when one can stop propagating a change – the Examiner should not confuse this with topological

criteria, such as ATRL and RTRL, disclosed in Abato. Page 16, line 6 to page 17, line 3 clearly lays out this distinction.

In view of the above, Abato fails to teach or suggest all the limitations of claim 17. Withdrawal of rejection of claim 17 is respectfully urged. Claims 18-32 depend from claim 17 are therefore believed to be in condition for allowance.

Claims 33, 34, and 35 are believed to be allowable at least for similar reasons set forth above with respect claim 17. Withdrawal of rejection of claim 33-35 is respectfully urged.

The specification has been amended to correct a minor typographical error. No new matter is added by way of this amendment.

This response is being filed with a one month extension of time. Please charge any fee deficiencies to IBM's deposit account shown on the cover sheet of this paper.

The undersigned is available for telephone consultation at any time.

Respectfully submitted,

Dated: May 26, 2006

By: _____

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